WHAT IS CLAIMED IS:

1. A thin film transistor structure for a field emission display, comprising:

a substrate having a semiconductor area for forming a thin film transistor;

a patterned poly-silicon layer having a source area, a drain area, and a channel on the semiconductor area of the substrate, wherein the source area and the drain area are doped with ions, and the channel is sandwiched in between the source area and the drain area;

a patterned first gate metal layer located on the poly-silicon layer;

a first gate-insulating layer sandwiched in between the poly-silicon layer and the first gate metal layer;

a patterned second gate metal layer located on the poly-silicon layer; and

a second gate-insulating layer sandwiched in between the poly-silicon layer and the second gate metal layer;

wherein the thickness of the second insulating layer is greater than that of the first gate-insulating layer, and the absolute voltage in the channel under the first gate metal layer is less than that under the second gate metal layer when a voltage higher than the threshold voltage thereof is applied to both of the first gate metal layer and the second gate metal layer.

2. The thin film transistor structure as claimed in claim 1, wherein the substrate is made of glass, plastic, quartz, silicon, or metal.

3. The thin film transistor structure as claimed in claim 1,

wherein the thin film transistor is a P-type MOS (metal-oxide-semiconductor) or an N-type MOS.

4. The thin film transistor structure as claimed in claim 1, wherein the first gate metal layer and the second gate metal layer are shorts or opens.

5. The thin film transistor structure as claimed in claim 1, wherein the projection of the first gate metal layer on the poly-silicon layer is discrete, overlapped, or contiguous with that of the second gate metal layer.

6. The thin film transistor structure as claimed in claim 1, wherein the projection of the first gate metal layer or the second gate metal layer on the poly-silicon layer is overlapped or non-overlapped with the source area and the drain area.

7. The thin film transistor structure as claimed in claim 1, wherein the source area connects to a capacitor that stores the informations for pixel, and the drain area connects to an electrode of a field emission display.

8. The thin film transistor structure as claimed in claim 7, wherein the capacitor, the first gate metal layer, and the second gate metal layer further connect to a drain electrode of a switch, and a source electrode of the switch connects to a data line of the field emission display; or the capacitor, the first gate metal layer, and the second gate metal layer further connect to the source electrode of the switch, and the drain electrode of the switch connects to the data line of the field emission display; and a gate

electrode of the switch connects to a scan line of the field emission display.

9. A method for manufacturing a thin film transistor of a field emission display, comprising:

(a) providing a substrate;

(b) forming a patterned poly-silicon layer on the substrate;

(c) forming a first gate-insulating layer;

(d) forming a patterned first gate metal layer;

(e) forming a second gate-insulating layer; and

(f) forming a patterned second gate metal layer;

wherein the thickness of the second insulating layer is greater than that of the first gate-insulating layer, and the absolute voltage in the channel under the first gate metal layer is less than that under the second gate metal layer when a voltage higher than the threshold voltage is applied to both of the first gate metal layer and the second gate metal layer.

10. The method as claimed in claim 9, wherein the substrate is made of glass, plastic, quartz, silicon, or metal.

11. The method as claimed in claim 9, wherein the thin film transistor is a P-type MOS (metal-oxide-semiconductor) or an N-type MOS.

12. The method as claimed in claim 9, wherein the first gate metal layer and the second gate metal layer are shorts or opens.

13. The method as claimed in claim 9, wherein the projection of the first gate metal layer on the poly-silicon layer is discrete, overlapped, or contiguous with that of the second gate metal layer.

14. The method as claimed in claim 9, further comprising a step of (d1) or (e1) forming a patterned source area and drain area in the poly-silicon layer after step (d) or (e), respectively.

15. The method as claimed in claim 14, wherein the source area and the drain area are ion-doped through ion implantation.

16. The method as claimed in claim 14, further comprising a step of (e2) forming a plurality of contact holes on the source area, drain area, or the gate metal layer by photolithography and etching processes after step (e1), thereby forming a plurality of electrically conductive lines that connects the source area, drain area, or the gate metal layer simultaneously with forming the second gate metal layer in step (f).

17. The method as claimed in claim 14, wherein the projection of the first gate metal layer or the second gate metal layer on the poly-silicon layer is overlapped or non-overlapped with the source area and the drain area.

18. The method as claimed in claim 9, further comprising a step of (g) forming a passivation layer on the thin film transistor after step (f).

19. The method as claimed in claim 18, further comprising a step of (h) forming an ITO layer after step (g).